

Laboratory 4

(Due date: **002**: March 25th, **003**: March 26th)

OBJECTIVES

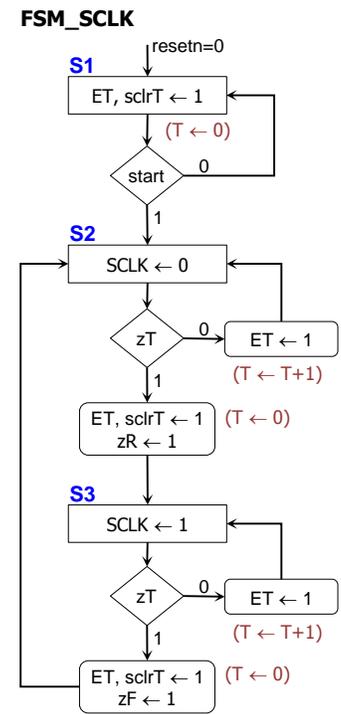
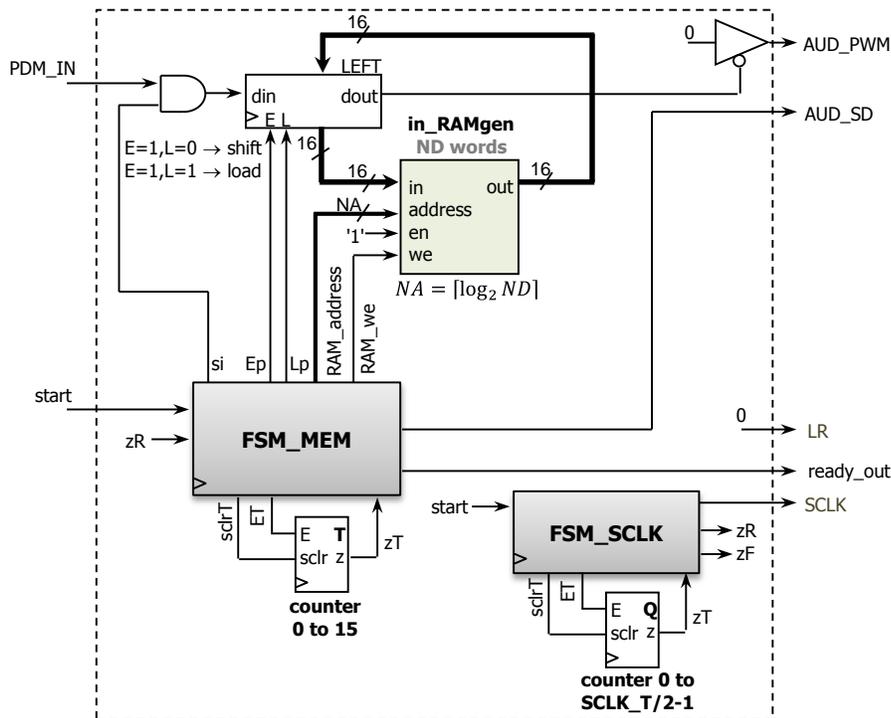
- ✓ Implement a Digital System: Control Unit and Datapath.
- ✓ Learn about reading PDM-coded input audio and playback PDM-coded output audio.
- ✓ Learn interfacing with MEMS microphones (that generate PDM signals) and using BlockRAMs in FPGAs.

VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a tutorial and a list of examples.

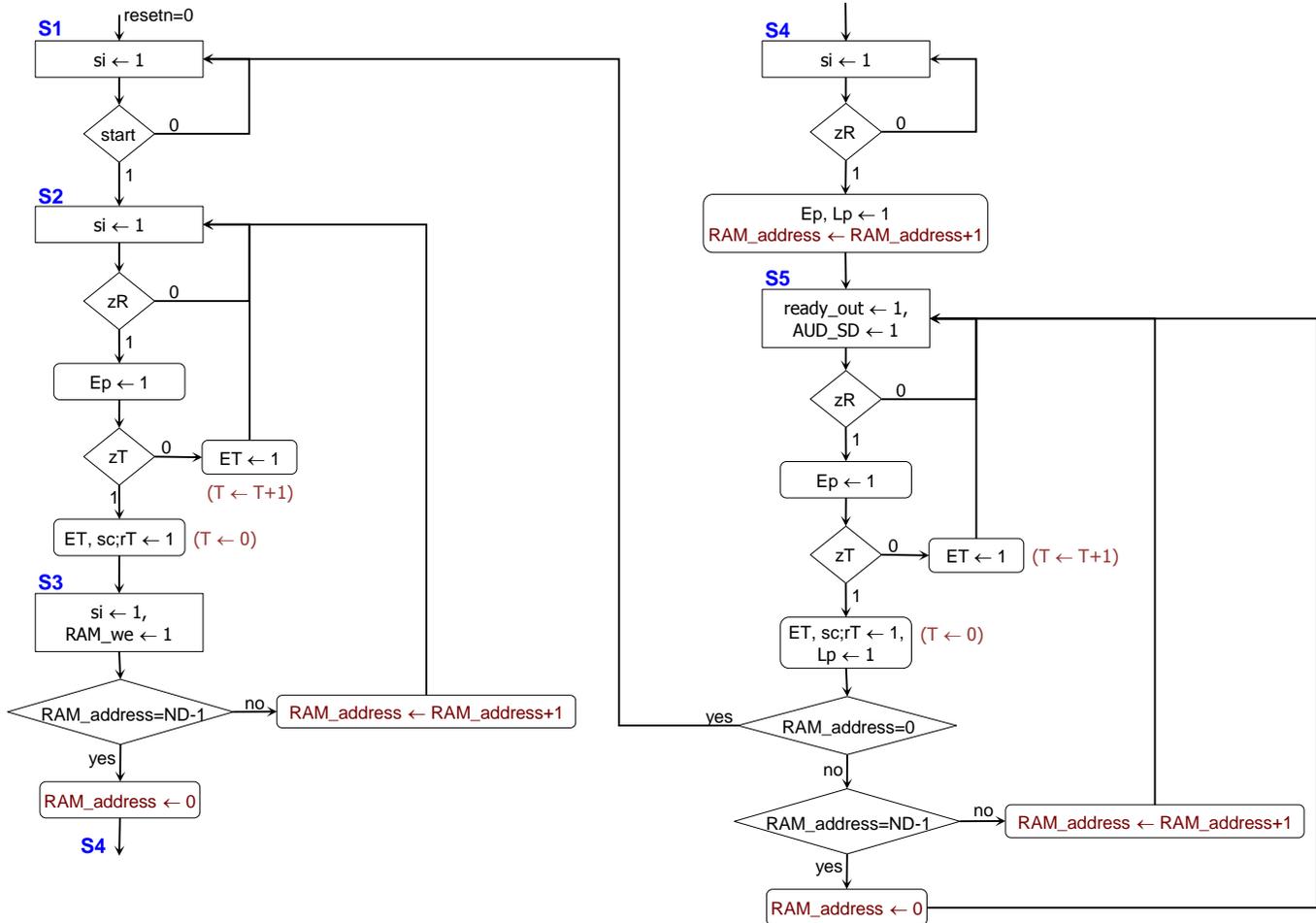
FIRST ACTIVITY: AUDIO RETRIEVAL AND PLAYBACK CIRCUIT (100/100)

- **MICROPHONE AND MONO AUDIO OUTPUT:** Implement the following circuit that reads data from the ADMP421 MEMS microphone, stores data in memory and plays data back on a mono audio output.



- **MEMS MICROPHONE (ADMP421):**
 - ✓ SCLK: 1 – 3 MHz. We use 1.2 MHz.
 - ✓ PDM_IN: PDM signal generated by the ADMP421.
 - ✓ LR: Left right control for stereo mode. We use LR = 0 (Data is captured on CLK rising edge).
- **MONO AUDIO OUTPUT:**
 - ✓ As stereo output is not supported, we only retrieve a mono audio input from the ADMP42 microphone (e.g. L/R = 0).
 - ✓ The on-board audio jack of the Nexys-4 DDR Board is driven by a low-pass filter with 12 KHz cut-off frequency. We provide a PDM signal (AUD_PWM: open-drain output) as input.
- **FSM_SCLK:**
 - ✓ This generates a free running clock (SCLK). It also generates a pulse on zR when a rising edge on SCLK occurs. We want to use a frequency of 1.2 MHz. This requires $SCLK_T=84$. You can use the VHDL code `fsm_sclk.vhd` (along with `my_genpulse_sclr.vhd`) with the parameter `COUNT_SCKLHP = SCLK_T/2=42`.
- **MEMORY:** Implemented with the on-chip memory (BlockRAMs) inside the Artix-7 FPGA.
 - ✓ Data requested or to be written is available on the next clock cycle. Use the given VHDL code `in_RAMgen.vhd`. This is a 2D memory of `nrows×ncols`. Word length: 16 bits. We can use it as a 1D memory by making `ncols=1`. Use the following parameters `nrows=512*512`, `ncols=1`, `INIT_VALUES="NO"`, `FILE_IMG ="myinival.txt"`.

- **FSM_MEM:** This is the main controller. $ND = 512 \times 512 = 2^{18}$. This FSM embeds the counter `RAM_address`.
 ✓ Duration of the sequence: $2^{18} \times 16 \times 84 \times 10ns = 3.52 \text{ seconds}$.



- **VIVADO DESIGN FLOW FOR FPGAs – NEXYS A7-100T** (*A7-50T: use `nrows=512*256` as there is less memory)
 - ✓ Create a new Vivado Project. Select the **XCA100T-1CSG324 Artix-7 FPGA** device.
 - ✓ Write the VHDL for the given circuit. Synthesize your circuit. (Run Synthesis).
 - ✓ With a 100 MHz input clock, write the VHDL testbench.
 - To avoid long simulation times, use `ncols=4x4`, `nrows=1` and `COUNT_SCLKHP = SCLK_T/2 = 2` for simulation purposes (resynthesize your circuit).
 - Generate the following input stream (4x4 16-bit words) to be captured at the rising edge of SCLK: 1110 1100 1110 1011 0100 0111 0001 0000 1010 1100 1110 1101 1110 1010 0101 0001 and then just 1's. The 16-bit values stored in memory should be: ECEB 4710 ACED EA51 FFFF ... FFFF. Verify that these values appear on the memory output on state S5. Place the `state` and `RAM_address` on the Simulator Wave Window. Run the simulation for 21 us.
 - ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**
 - ✓ I/O Assignment: Create the XDC file. Use `CLK100MHZ` for the input `clock`, `CPU_RESET` push button for `resetn`, `LED0` for `ready_out`, `BTNC` for `start`, `M_CLK` for `SCLK`, `M_DATA` for `PDM_IN`, `M_LRSEL` for `LR`, `AUD_PWM` for `AUD_PWM`, `AUD_SD` for `AUD_SD`.
 - ✓ Implement your design (Run Implementation).
 - ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
 - ✓ Generate and download the bitstream on the FPGA. Test the circuit: press `start` and record an audio sequence for 3.52 seconds. After that, the audio sequence is played back (use a headphone/speaker). **Demonstrate this to your TA.**
- Submit (as a .zip file) the generated files: VHDL code, and VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____

Date: _____